Confirmation no. 9258 PATENT

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant:	SANDULEANU	Examiner:	Perez, J.
Serial No.:	10/533,058	Group Art Unit:	2611
Filed:	April 27, 2005	Docket No.:	NL021079US
Title:	PLL USING UNBALANCED QUADRICORRELATOR		

APPEAL BRIEF

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Commissioner For Patents
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Dear Sir:

This Appeal Brief is submitted pursuant to 37 C.F.R. §41.37, in support of the Notice of Appeal filed December 5, 2008 and in response to the rejections of claims 1-7 as set forth in the Final Office Action dated July14, 2008.

Please charge Deposit Account number 50-0996 (NXPS.466PA) $540.00 for filing this brief in support of an appeal as set forth in 37 C.F.R. §1.17(c). If necessary, authority is given to charge/credit Deposit Account 50-0996 additional fees/overages in support of this filing.

I. Real Party In Interest

The real party in interest is NXP Semiconductors. The application is presently assigned of record, at reel/frame nos. 017244/0842 to NXP, B.V., headquartered in Eindhoven, the Netherlands.

II. Related Appeals and Interferences

While Appellant is aware of other pending applications owned by the above-identified Assignee, Appellant is unaware of any related appeals, interferences or judicial proceedings that would have a bearing on the Board's decision in the instant appeal.

III. Status of Claims

Claims 1-7 stand rejected and are presented for appeal. Claims 8-9 have been allowed. A complete listing of the claims under appeal is provided in an Appendix to this Brief.

IV. Status of Amendments

No amendments have been filed subsequent to the Final Office Action dated July 14, 2008.

V. Summary of Claimed Subject Matter

Appellant's invention is related to a Phase Locked Loop (PLL) having a frequency detector with an unbalanced quadricorrelator that can be useful for mitigating problems associated with digital implementations, such as delays from combinatorial logic.

Commensurate with independent claim 1, an example embodiment of the present invention is directed to a Phase Locked Loop (PLL) comprising a frequency detector including an unbalanced quadricorrelator, the quadricorrelator comprising a frequency detector (FIG. 2, outputs FD- and FD+ and page 4:24-27) including double edge clocked bi-stable circuits (FIG. 2, elements 21-24 and pages 3:31-4:7) coupled to a first multiplexer (FIG. 2, element 31 or 32 and pages 3:31-4:7) and to a second multiplexer (FIG. 2, element 31 or 32 and pages 3:31-4:7) being controlled by a signal having a same bitrate as the incoming signal, and a phase detector (FIG. 2 element DFF and page 4:19-21) controlled by

a first signal pair provided by the first multiplexer (FIG. 2, signal pairs PQ or PI) and by a second signal pair (FIG. 2, signal pairs PQ or PI) provided by the second multiplexer.

As required by 37 C.F.R. § 41.37(c)(1)(v), a concise explanation of the subject matter defined in the independent claims involved in the appeal is provided herein. Appellant notes that representative subject matter is identified for these claims; however, the abundance of supporting subject matter in the application prohibits identifying all textual and diagrammatic references to each claimed recitation. Appellant thus submits that other application subject matter, which supports the claims but is not specifically identified above, may be found elsewhere in the application. Appellant further notes that this summary does not provide an exhaustive or exclusive view of the present subject matter, and Appellant refers to the appended claims and their legal equivalents for a complete statement of the invention.

VI. Grounds of Rejection to be Reviewed Upon Appeal

The grounds of rejection to be reviewed on appeal are as follows:

A. Claims 1-2 and 5-6 stand rejected under 35 U.S.C. § 103(a) over the Moser reference (U.S. Patent No. 6,853,696) in view of the Savoj reference ("Design of Half-Rate Clock and Data Recovery Circuits for Optical Communications Systems").

B. Claims 3-4 stand rejected under 35 U.S.C. § 103(a) over the Moser reference in view of the Savoj reference and further in view of the Morgan reference (U.S. Patent No. 6,320,406).

C. Claim 7 stands rejected under 35 U.S.C. § 103(a) over the Moser reference in view of the Savoj reference and further in view of the Lee reference (U.S. Patent No. 5,734,301).

VII. Argument

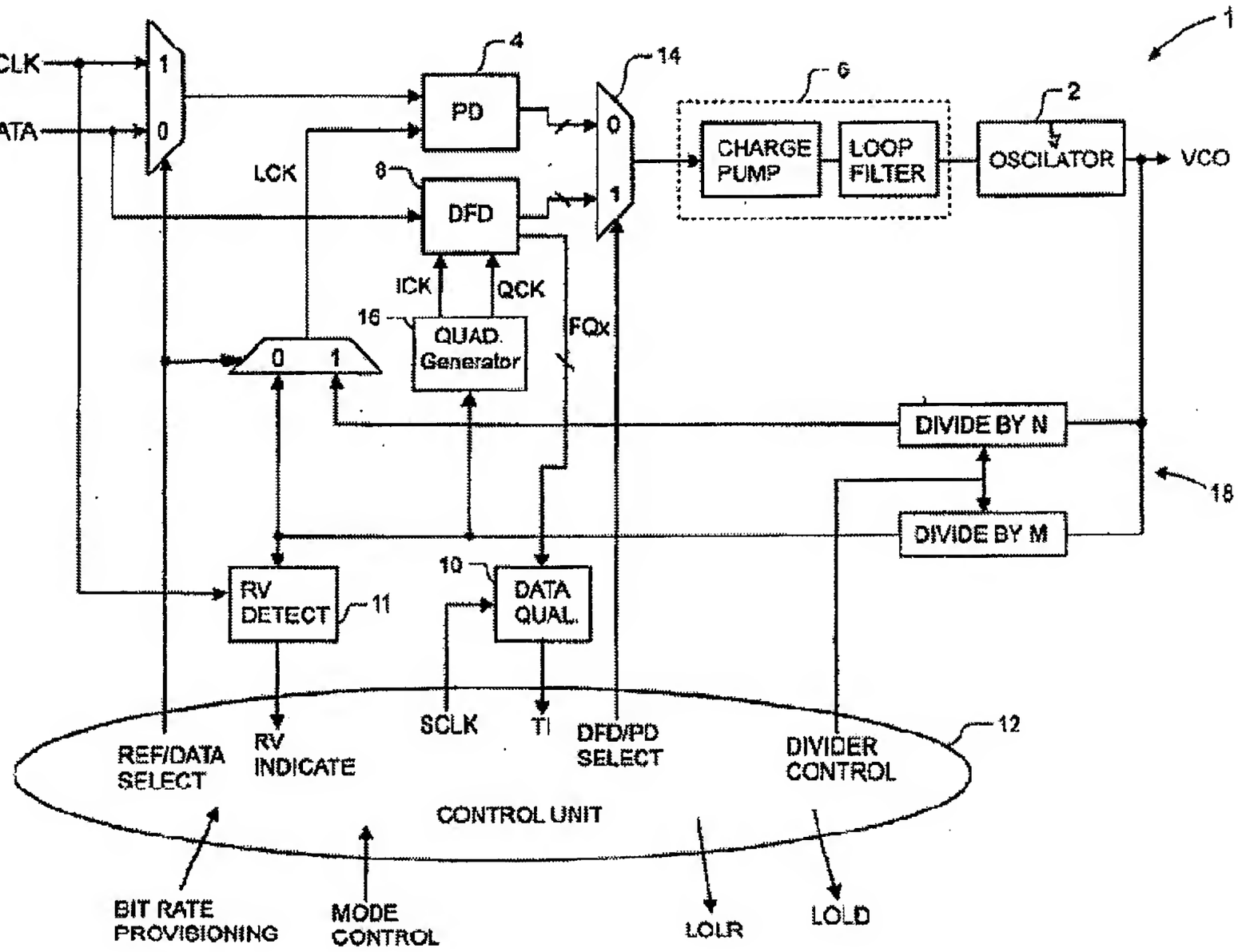
A. Overview

A main first issue addressed in this Appeal is the Examiner's flawed reasoning that a phase detector is equivalent to a frequency detector and that such assertion, by itself, is sufficient for a § 103 rejection. As will be discussed in more detail hereafter, the record conclusively shows that a phase detector is not equivalent to a frequency detector, technically or for the limited purposes of patentability. Moreover, it is well established law that an assertion of equivalency is insufficient to deny patentability. *See e.g.*, *In re Ruff*, 45 C.C.P.A. 1037, 1048 (C.C.P.A. 1958), "That two things are actually equivalents, in the sense that they will both perform the same function, is not enough to bring into play the rule that when one of them is in the prior art the use of the other is obvious and cannot give rise to patentable invention." Here, the Examiner has improperly based the equivalency argument upon Appellant's specification. Accordingly, the Examiner's rejection is improper for reasons independent of whether there is actual equivalency.

Among other important issues, this Appeal addresses the rejections for lack of an adequate reason for the asserted combination, and the record shows that the references teach away from the combination.

It is important to understand that the primary reference (Moser) teaches that selective control over a phase detector and a frequency detector provides benefits to the circuit, and thereby supports the well-known fact that a phase detector and a frequency detector are significantly different. For convenience, FIG. 1 of the primary reference is reproduced below.

FIG. 1



The primary reference teaches that a multiplexor (14) allows for selective use of either a phase detector (PD 4) or a frequency detector (DFD 8). In particular, when the incoming signal is out of the pull-in range of the phase detector (PD 4), the frequency detector (DFD 8) is used (*see, e.g.*, Moser at Col. 6:31-41). Thus, the primary reference is explicit in the delineation between a phase detector and a frequency detector and teaches the benefit of providing separate frequency and phase detection. Notwithstanding, the Examiner has taken the contrary position that a frequency detector and a phase detector are functionally equivalent (*see, e.g.*, Final Office Action of July 14, 2008 at page 2). The Examiner has also taken the position that frequency detector 8 is a phase detector (*see, e.g.*, Advisory Action of November 17, 2008 at page 2).

The Examiner acknowledges that if a frequency detector and a phase detector are functionally equivalent, there is no basis for the rejection because there is no correspondence. As shown below, the record, which includes the cited references and Appellant's specification, explicitly contradicts the Examiner's assertion of equivalency.

B. The Rejection Of Claims 1-2, 5-6 Under § 103(A) Over The Moser Reference In View Of The Savoj Reference Is Improper Because Correspondence Has Not Been Shown For Each Claim Limitation.

The claim limitations directed to specific arrangements of circuit elements that include a frequency detector containing a phase detector. To address these limitations, the Examiner alleges that the frequency detector of the primary (Moser) reference is the same as a phase detector and then attempts to modify this mislabeled detector with elements from the secondary (Savoj) reference. While the Examiner's argument of equivalency has little merit (as discussed in more detail below), it is well established that an assertion of functional equivalency cannot preclude patentability. *See e.g.*, *In re Ruff*, 45 C.C.P.A. 1037, 1048 (C.C.P.A. 1958), "That two things are actually equivalents, in the sense that they will both perform the same function, is not enough to bring into play the rule that when one of them is in the prior art the use of the other is obvious and cannot give rise to patentable invention." To establish equivalency, the Examiner has improperly relied upon Appellant's Specification. For example, the Final Office Action of July 14, 2008 at page 2 states "Furthermore in the applicant's specification the phase detector of the quadricorrelator only outputs frequency error." While this statement is untrue, the issue does not turn only on the validity of the statement because equivalency gleaned from Appellant's Specification cannot be used to deny patentability. Rather, the prior art must be used to establish such a proposition. Accordingly, the Examiner has not presented a *prima facie* case of obviousness because the Examiner cannot assert correspondence through an assertion of functional equivalency that is based on a statement from Appellant's Specification.

Moreover and contrary to the position of the Examiner, the skilled artisan would readily understand that, especially in phase-locked-loop (PLL) circuits, a frequency detector is not at all equivalent to a phase detector. The frequency of a signal is the number of occurrences (*e.g.*, signal transitions) in a given time period. The phase of two signals is the angular difference between the signals (*e.g.*, the time based relationship between similar reference points in the periodic function of the signals). Accordingly, a frequency detector provides an output that directly indicates the difference in frequency between two signals, and a phase detector provides an output that directly indicates the angular difference between two signals. These definitions are fully supported by the record, which includes Appellant's

Specification (*see, e.g.*, Specification (as originally filed) page 4:9-30) and the relied upon references (*see, e.g.*, Moser, col. 6:30-41 and Savoj, page 122, Section 2.21, last paragraph "The ideal is that the fine control is established by the phase detector and the coarse control is a provision for adding a frequency detection loop.").

The Examiner has erroneously asserted that a component identified by the primary reference as being a frequency detector is equivalent to a phase detector (*see, e.g.*, Advisory Action of November 17, 2008 at page 2). The Examiner purports to support this erroneous conclusion with teachings of the primary reference which state that frequency information correlates to phase relationship (*see* Advisory Action of November 11, 2008, page 2 "FQ1 and FQ2 gives correlative information about the phase relationship"). Indeed, frequency and phase relationships of two signals have some correlation (*i.e.*, mismatches in frequencies can cause the phase relationship to change over time). It is not logical, however, to conclude that because there is a correlation between frequency and phase that the two are therefore identical. The skilled artisan, either before or after reading the references of record, would have readily understood the differences between frequency and phase. Thus, the skilled artisan would not have equated a frequency detector with a phase detector.

Moreover, the Examiner's asserted combination includes a replacement of components relied upon to show correspondence. More specifically, the Examiner erroneously asserts that elements 38, 34a and 34b of FIG. 2 of the primary reference correspond to a phase detector. These components are part of frequency detector 8 of FIG. 1 of the primary reference. The secondary reference teaches a completely different circuit for implementing a frequency detector that does not include elements 38, 34a and 34b of FIG. 2 of the primary reference. Thus, the asserted combination is further improper because the correspondence relies upon elements that are being replaced as part of the combination.

The Examiner's rejection requires this improper blurring of the distinctions between phase and frequency to show correspondence. The Examiner's rejection also relies upon elements of the primary reference while subsequently replacing these elements with elements from the secondary reference. Accordingly, the rejection is improper for failing to show correspondence to each claim limitation and should be reversed.

C. The Rejection Of Claims 1-2 And 5-6 Under 35 U.S.C. § 103(A) Over The Moser Reference In View Of The Savoj Reference Is Improper Because There Is No Valid Reason For The Asserted Combination.

There is no proper reason to combine the primary reference (Moser) and secondary reference (Savoj), and the Examiner's explanation is illogical as it would not yield an operable circuit consistent with the purpose of the primary reference. As explained at M.P.E.P. § 2143.01, a §103 rejection cannot be maintained when the asserted modification undermines purpose of main reference. The M.P.E.P. and the applicable U.S. Supreme Court law requires that the claim be considered "as a whole" (35 U.S.C. §103(a)), while taking into consideration the problem(s) being addressed by the claimed invention and any unexpected results. Thus, the Supreme Court in *KSR* reaffirmed the familiar framework for determining obviousness as set forth in *Graham v. John Deere Co.* (383 U.S. 1, 148 USPQ 459 (1966)), and stated that, "when the prior art teaches away from combining certain known elements, discovery of a successful means of combining them is more likely to be non-obvious." The Court further tied in the relationship between the teach-away standard and demonstrating unpredictable results. "The fact that the elements [in *Adams*] worked together in an unexpected and fruitful manner supported the conclusion that Adam's design was not obvious to those skilled in the art." *KSR Int'l Co. v. Teleflex, Inc.*, 127 S. Ct. 1727, 1742 (2007). The Examiner has addressed the teachings of the reference that would lead away from the asserted combination nor as the Examiner provided a logical reason for the asserted combination.

For example, Savoj teaches using multiple phase detectors to implement a combined phase and frequency detection circuit, whereas the primary reference explicitly separates frequency detection from phase detection using a multiplexer that selects the output of either the frequency detector (DFD) or the phase detector (PD), but not both. Moreover, the primary reference explicitly states that the frequency detector does not include a phase detection function. The primary reference teaches that it is desirable to use frequency detection and phase detection separately. For example, when the data rates fall outside of the pull-in range of the phase detector, a frequency detector is used. (*see, e.g.*, Moser at Col. 6, lines 31-42). Combining these aspects would contradict the intended operation of the primary reference,

which is directed to a clock recovery unit that uses both a frequency detector and a phase detector (*see, e.g.*, Moser at Col. 6, lines 12-29).

The stated reason for the combination is "in order to provide an improved performance in frequency detector in order to utilize a wider range of frequencies…". Respectfully, this stated reason is unrelated to the proposed modification. While a wider range of frequencies might be desirable in some applications, this is an aspect taught to be provided by the ring oscillator. More specifically, the Examiner's stated reason for implementing the proposed combination is consistent with a quotation from the secondary reference regarding benefits seen from "a three-stage ring oscillator to achieve wide tuning range" (Svaoj, page 121, Introduction). The Examiner is improperly inferring benefits from the ring oscillator to that of the frequency detector. Thus, the comparison of an improved performance between the primary reference and the asserted combination is without merit.

For the aforementioned reasons, there is no remaining reason for the skilled artisan to implement the proposed combination of references. Accordingly, the rejection cannot stand and should be reversed.

D. The Rejection Of Claims 3-4 Under 35 U.S.C. § 103(A) Over The Moser Reference In View Of The Savoj Reference And Further In View Of The Morgan Reference Is Improper For Each Of The Reasons Presented Above.

Claims 3-4 depend from claim 1 and necessarily contain the limitations thereof. The addition of aspects from the Morgan reference do not cure (and are not alleged by the Examiner to cure) the deficiencies identified in Sections A, B and C above. Accordingly, the rejection is improper for these same deficiencies and should be reversed.

E. The Rejection Of Claim 7 Under 35 U.S.C. § 103(A) Over The Moser Reference In View Of The Savoj Reference And Further In View Of The Lee Reference Is Improper For Each Of The Reasons Presented Above.

Claim 7 depends from claim 1 and necessarily contains the limitations thereof. The addition of aspects from the Lee reference does not cure (and is not alleged by the Examiner to cure) the deficiencies identified in Sections A, B and C above. Accordingly, the rejection is improper for these same deficiencies and should be reversed.

VIII. Conclusion

In view of the above, Appellant submits that the rejections of claims 1-7 are improper and therefore requests reversal of the rejections as applied to the appealed claims and allowance of the entire application.

Authority to charge the undersigned's deposit account was provided on the first page of this brief.

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APPENDIX OF CLAIMS INVOLVED IN THE APPEAL
(S/N 10/533,058)

1. A Phase Locked Loop comprising a frequency detector including an unbalanced quadricorrelator, the quadricorrelator comprising a frequency detector including double edge clocked bi-stable circuits coupled to a first multiplexer and to a second multiplexer being controlled by a signal having a same bitrate as the incoming signal, and a phase detector controlled by a first signal pair provided by the first multiplexer and by a second signal pair provided by the second multiplexer.

2. A Phase Locked Loop as claimed in claim 1, wherein the frequency detector comprises a first pair of double edge clocked bi-stable circuits coupled to the first multiplexer, and a second pair of double edge clocked bi-stable circuits coupled to the second multiplexer, which first and second pairs are supplied by mutually quadrature phase shifted signals respectively to provide the first signal pair and the second signal pair indicative for a phase difference between the incoming signal and mutually quadrature phase shifted signals.

3. A Phase Locked Loop as claimed in claim 1, wherein the phase detector comprises a D flip-flop receiving the first signal pair and being clocked by the second signal pair, the second signal pair being inputted to respective gates of a first transistors pair for determining a state ON or OFF of a current through said first transistors pair.

4. A Phase Locked Loop as claimed in claim 3, wherein current through the first transistor pair biases a second transistor pair, the second transistor pair receiving the first signal pair and generating an output signal indicative for a frequency error between the incoming data signal and Clock signals.

5. A Phase Locked Loop as claimed in claim 2, wherein the mutually quadrature phase shifted signals are generated by a voltage controlled oscillator.

6. A Phase Locked Loop as claimed in 5, wherein a frequency error signal produced by the quadricorrelator is inputted to a coarse control input of the voltage controlled oscillator via a first charge pump coupled to a first low-pass filter coupled to an adder.

7. A Phase Locked Loop as claimed in claim 6, wherein a fine control input is controlled by a signal provided by a phase detector coupled to a second charge pump coupled to second low-pass filter.

APPENDIX OF EVIDENCE

(S/N 10/533,058)

Appellant is unaware of any evidence submitted in this application pursuant to 37 C.F.R. §§ 1.130, 1.131, and 1.132.

APPENDIX OF RELATED PROCEEDINGS

(S/N 10/533,058)

As stated in Section II above, Appellant is unaware of any related appeals, interferences or judicial proceedings.